What is claimed is:

1. A data processing control apparatus that alternatively makes one among a plurality of service executers each designed to execute predetermined service execute service, comprising:

a controller for performing control so that whichever of the service executers requested to execute service is given a highest order of priority executes service;

a priority updater for updating orders of priority given to the individual service executers in such a way that, every time a given service executer has continuously executed an amount of service that a single service executer is permitted to continuously execute, the given service executer is given a lowest order of priority; and

a memory for storing, for each of the service executers, data indicating amount of service that a single service executer is permitted to continuously execute.

2. A DMA controller comprising:

a setting register for permitting a CPU to make settings for DMA transfer therein;

an operation register for permitting data stored in the setting register to be written thereto, or an operation counter for performing counting operation by use of the data;

an operation controller for performing control so that, when DMA transfer is started, the data stored in the setting register is written to the operation register or the operation counter; and

a transfer executer for executing DMA transfer based on the data stored in the operation register or the operation counter.

3. A DMA controller comprising:

an operation register for storing transfer conditions under which DMA transfer is currently being executed;

a setting register for storing transfer conditions under which DMA transfer is to be executed next time;

a setting execution register for storing transfer conditions under which to transfer, by DMA transfer, transfer conditions for DMA transfer from an external memory to the setting register;

a selector for alternatively selecting one of the setting register and the setting execution register;

a selection controller for performing control so that the register selected by the selector is switched alternately between the setting register and the setting execution register every time DMA transfer ends;

an operation register controller for performing control so that, when DMA transfer is started, data stored in the register selected by the selector is written to the operation register; and

a transfer executer for executing DMA transfer based on the data stored in the operation register.

4. A data processing apparatus comprising a CPU for executing a program and a memory for storing data or for storing data and the program wherein

the data can be read out from the memory through a data processing control apparatus,

the data processing control apparatus alternatively making one among a plurality of service executers each designed to execute predetermined service execute service,

the data processing control apparatus comprising:

a controller for performing control so that whichever of the service executers requested to execute service is given a highest order of priority executes service;

a priority updater for updating orders of priority given to the individual service executers in such a way that, every time a given service executer has continuously executed an amount of service that a single service executer is permitted to continuously execute, the given service executer is given a lowest order of priority; and

a memory for storing, for each of the service executers, data indicating amount of service that a single service executer is permitted to continuously execute.

5. A data processing apparatus comprising a CPU for executing a program and a memory for storing data or for storing data and the program wherein the data can be read out from the memory through a DMA controller,

the DMA controller comprising:

a setting register for permitting a CPU to make settings for DMA transfer therein;

an operation register for permitting data stored in the setting register to be written thereto, or an operation counter for performing counting operation by use of the data;

an operation controller for performing control so that, when DMA transfer is started, the data stored in the setting register is written to the operation register or the operation counter; and

a transfer executer for executing DMA transfer based on the data stored in the operation register or the operation counter.

6. A data processing apparatus comprising a CPU for executing a program and a memory for storing data or for storing data and the program wherein the data can be read out from the memory through a DMA controller,

the DMA controller comprising:

an operation register for storing transfer conditions under which DMA transfer is currently being executed;

a setting register for storing transfer conditions under which DMA transfer is to be executed next time;

a setting execution register for storing transfer conditions under which to transfer, by DMA transfer, transfer conditions for DMA transfer from an external memory to the setting register;

a selector for alternatively selecting one of the setting register and the setting execution register;

a selection controller for performing control so that the register selected by the selector is switched alternately between the setting register and the

setting execution register every time DMA transfer ends;

an operation register controller for performing control so that, when DMA transfer is started, data stored in the register selected by the selector is written to the operation register; and

a transfer executer for executing DMA transfer based on the data stored in the operation register.